Common Mistakes in Power-Supply Layouts and How to Avoid Them

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The physical layout is just as critical to the performance of your power-supply design as the selection of the semiconductor devices or surrounding passive components.

Introduction

Poor layout increases the parasitic inductance, capacitance and resistance within the circuit. It can increase noise pickup between different parts of the circuit, and increase thermal stresses within the regulator.

The synchronous buck converter topology shown in **Figure 1** illustrates where in the circuit parasitic inductance has the most detrimental effect (for example, the input capacitor loop) and also where the inductance is tolerable, with fewer ill effects. A poor layout will generate parasitic inductance first though excess track lengths, and second where connections exist between layers using vias. It is important to minimize parasitic inductance in critical areas.

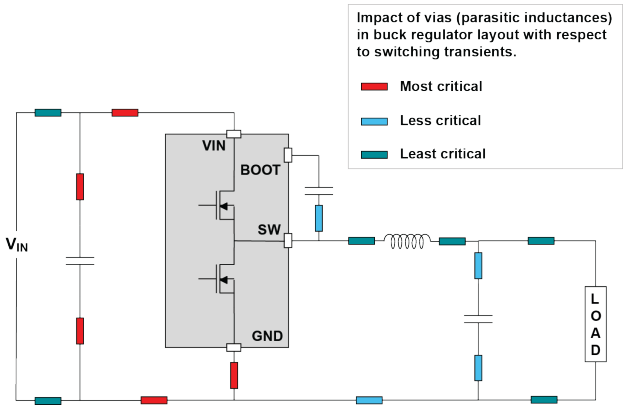

Figure 1. *The impact of parasitic inductance in a buck regulator layout.*

The symptoms resulting from a nonoptimized layout include poor regulation, output instability, excess output ripple and noise, electromagnetic interference (EMI) issues, poor thermal performance, and a reduction in lifetime and reliability. Fixing issues after the fact may require additional components such as snubbers or ferrite beads, or even a complete printed circuit board (PCB) redesign, leading to increased costs and delays. The goal is that some of the examples in this paper will help you avoid these costly mistakes [1],[2].

Input Capacitor Placement

Figure 2 shows the switch-node waveform and output ripple for a 12-V to 1.2-V, 8-A DC/DC regulator using the Texas Instruments (TI) **TPS56C215** integrated synchronous buck regulator [3]. The switch-node waveform exhibits significant ringing, peaking at approximately 17 V. This high-frequency ringing will increase EMI and contribute to the high output voltage ripple. In addition, the maximum recommended switch voltage for this device is 17 V with an absolute maximum of 19 V, so the ringing is likely to put overvoltage stress on the switch.

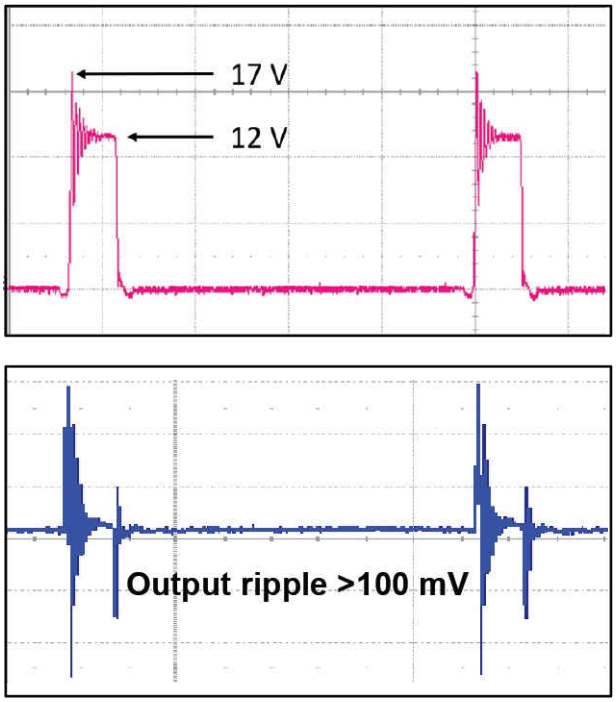

Figure 2. *Switch node (top) and output ripple (bottom) waveforms for poor input capacitor placement.*

The highest switching currents in a buck-converter circuit flow in the input capacitor loop. Any parasitic inductance in this loop can lead to ringing. **Figure 3** shows the original layout with the input capacitor positions highlighted in green and the red arrows indicating the input loop current path. The capacitors are some distance from the VIN and PGND pins and on the other side of the PCB, adding both track and via inductance into the loop.

Adding a snubber or bootstrap resistor to slow down the switching edges will reduce ringing, but the addition of either component reduces efficiency. **Figure 3** shows the identical circuit laid out on a single side of the PCB, with the input capacitors (again highlighted in green) placed directly next to the VIN and PGND pins of the device. This placement of the input capacitors greatly reduces the inductance in the loop; eliminates ringing on the switch node; and reduces the output ripple to about 4 mV, as shown in **Figure 4**. The peak switch voltage is more comfortably within the recommended range. Finally, reducing the ringing will decrease the EMI.

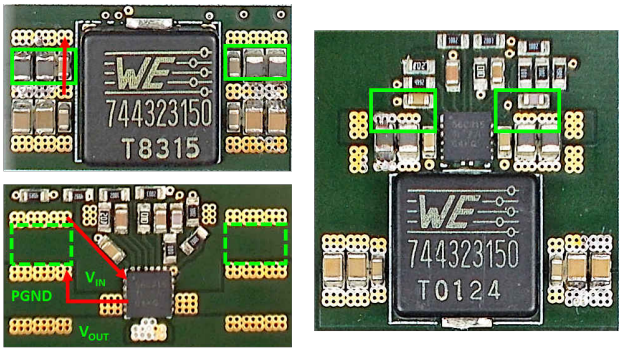

Figure 3. *Original double-sided layout (left); improved single-sided layout (right).*

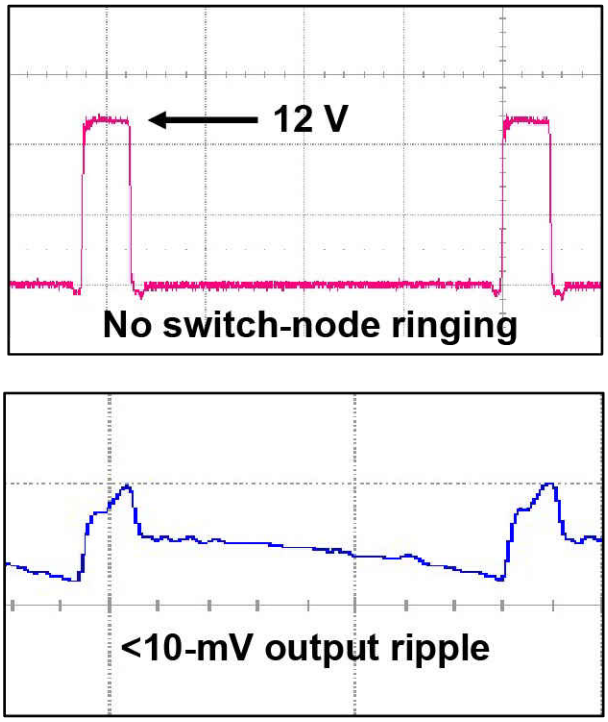

Figure 4. *Switch-node (top) and output ripple (bottom) waveforms for the correct input placement.*

It is good practice to add high-frequency bypass capacitors on the input to decouple the high-frequency harmonics found in the fast switching edges. Placing the high-frequency bypass capacitor closest to the VIN and PGND pins to minimize the track inductance ensures the absolute minimum amount of parasitic inductance in the high-frequency loop. The equivalent series inductance (ESL) of the capacitor is also important, so select small packages with low ESL.

Noise From an Unshielded Inductor

Figure 5 shows the output ripple of a 12-V to 2.5-V, 2.5-A synchronous buck converter using the **TPS563209** [4]. In this case, the output ripple in the upper plot is not excessive (approximately 24 mV, excluding spikes) but includes a suspicious square-wave component. De-soldering the inductor, rotating it 180° and refitting it causes an inverted square-wave component, as shown in the lower plot of **Figure 5**.

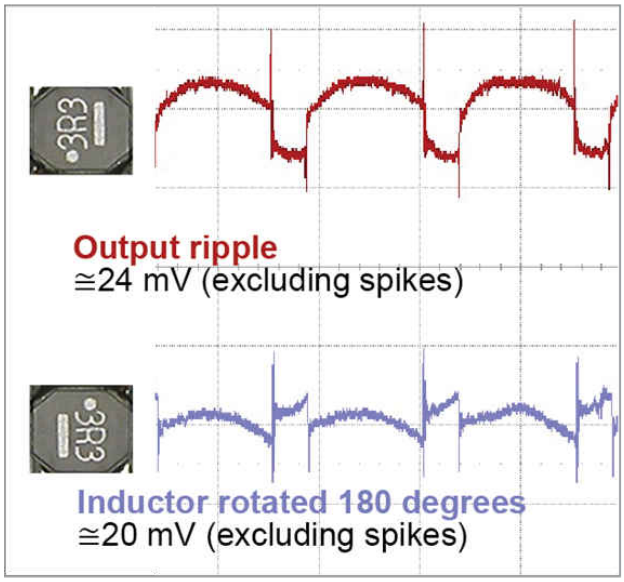

Figure 5. *Output ripple with square wave caused by magnetic field coupling.*

The inductor used here is a semishielded type, where an epoxy paste containing ferrite powder covers the windings. This paste offers only limited magnetic shielding. A semishielded inductor is not much different than an unshielded inductor [5]. This limited shielding means the magnetic field is not well contained and can spread beyond the edges of the inductor. In **Figure 6**, the single-sided layout has the output capacitors (in the green box) next to the inductor. The uncontained magnetic field from the inductor couples to the equivalent series inductance (ESL) of the adjacent output capacitor, which acts like a transformer and couples the switch-node waveform onto the output. Rotating the inductor reverses the current and thus the magnetic field, inverting the coupled waveform [6].

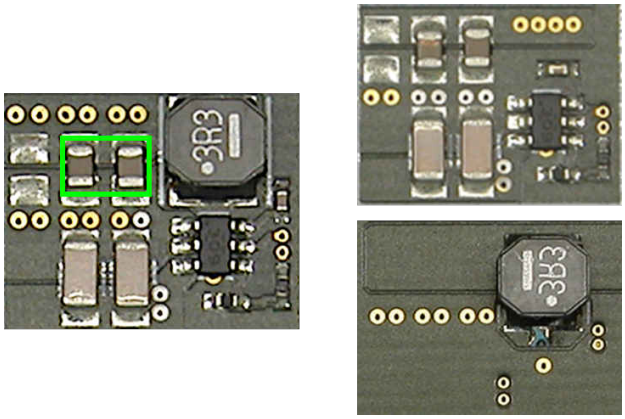

Figure 6. *Original single-sided layout (left); improved double-sided layout (right).*

Ensuring that the magnetic field from the inductor does not couple to the output capacitor ESL – either by containing the magnetic field using a fully shielded inductor or by moving the capacitor out of the magnetic field – can eliminate the square waveform. The areas labeled 2 and 3 in **Figure 7** illustrates moving the capacitor further away from the inductor or to the other side of the board, out of the plane of the magnetic field from the inductor.

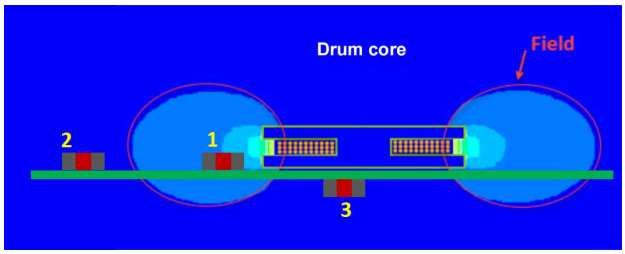

Figure 7. *Representation of the magnetic field of a semishielded inductor and interaction with nearby capacitors (Image courtesy of Coilcraft Inc.)*

The layout shown in **Figure 6**, with the inductor on the other side of the board from the capacitors, produces the output ripple shown in **Figure 8**. The square waveform is almost entirely eliminated, although spikes related to the switching edges are still present.

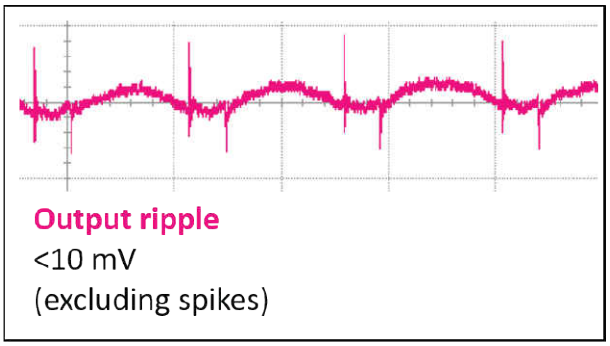

Figure 8. *Output ripple with square-waveform component eliminated.*

The main contributor to the spikes is the fast edge of the switch-node waveform coupling through the parasitic capacitance of the inductor. Selecting an inductor with the highest self-resonant frequency (SRF) minimizes the parasitic capacitances and reduces the amplitude of the spikes [7].

Place the inductor with the start of the winding (marked with a dot or bar) connected to the switch node. The start of the winding is buried in the center of the inductor. The outer windings that connect to the DC output, do provide some self-shielding.

It is also usually a good idea to have a ground plane under the inductor, as this provides some electric field shielding benefits that can reduce EMI. This ground plane will not do much for magnetic shielding, however. The skin depth in copper at typical switching frequencies would require an unreasonable thickness of copper to achieve even minimal magnetic shielding.

A Large High-Impedance Node

A **TPS565208** synchronous buck converter is generating a 1.05-V, 5-A output from 12 V. **Figure 9** shows the output voltage with >70 mV of noise and ripple, and the switching waveform exhibiting significant jitter. The output transient response stability is also affected.

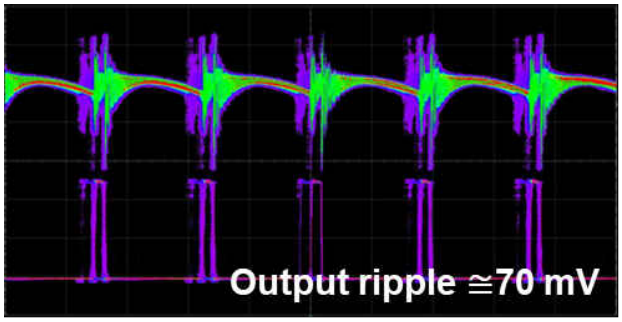

Figure 9. *Output voltage (top trace) with excess ripple and noise, and switching waveform (bottom trace) jitter.*

The feedback pin of a regulator is a high-impedance node and is very sensitive to noise. Keep the feedback node as small as possible, with the feedback resistors as close as possible to the feedback pin.

In **Figure 10**, the upper image shows the layout associated with the unstable output. The output resistors (highlighted in green) are placed close to the VOUT terminal; the track back to the high-impedance feedback node stretches across the board – past the inductor – and picks up noise. The bottom image in **Figure 10** shows a layout in which the resistors are moved close to the feedback pin and the feedback track is short and kept well clear of the inductor and switch node.

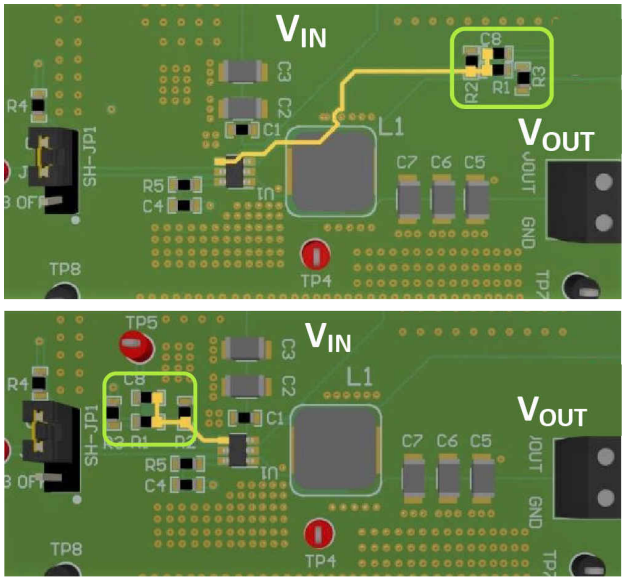

Figure 10. *Layout with long track connected to high-impedance feedback node (top); layout with feedback resistors closer to the feedback pin in order to minimize the feedback track length (bottom).*

The resulting output, shown in **Figure 11**, is much cleaner, with ripple reduced to approximately 20 mV and little or no evidence of jitter on the switching waveform.

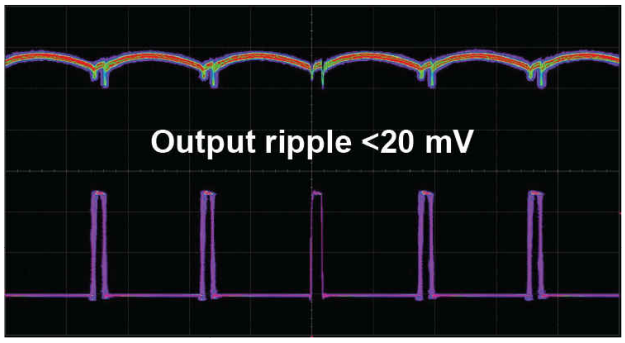

Figure 11. *Minimizing the feedback track reduces ripple and eliminates jitter.*

Avoid running sensitive signals under the inductor or switch node wherever possible. That includes the regulator feedback, but also any other signals in the circuit that could be susceptible to noise.

Where the load is some distance from the regulator, consider a differential connection, as shown in **Figure 12**. Some devices such as the **TPS548B27** have a difference amplifier included, or you could implement an external amplifier. Run the feedback and remote ground connections next to each other to ensure that any noise is coupled onto both equally and is then rejected by the difference amplifier [8].

When selecting feedback resistor values, high values maximize efficiency because less current is drawn through the resistors. High resistor values are more susceptible to noise, however, and can allow small feedback bias currents to shift the output voltage. A total feedback resistance in the range of 10 kΩ to 100 kΩ is usually a good compromise.

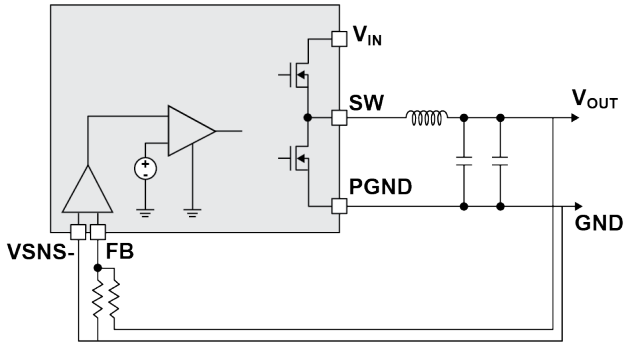

Figure 12. *Using a difference amplifier to implement differential remote sensing.*

Output Voltage-Sense Measurements

The **TPS543C20** synchronous buck converter can generate well-regulated output voltages capable of high-current loading. **Figure 13** shows a design meant to have a 0.85-V output that can accept loads as high as 20 A. The output voltage is sensed directly. In **Figure 13**, the trace highlighted in cyan shows the connection to the output voltage.

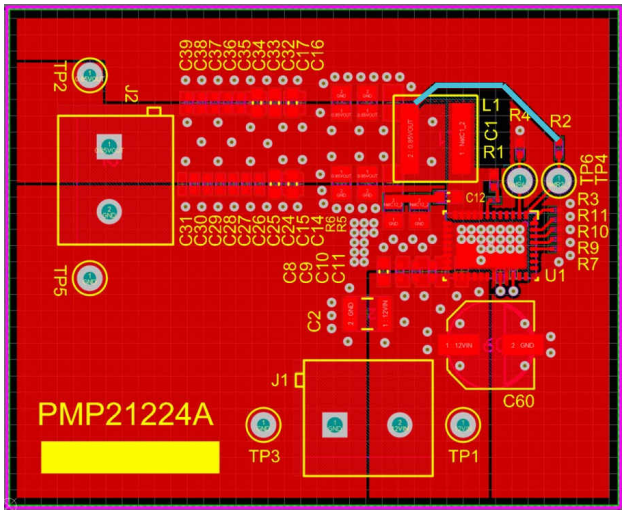

Figure 13. *20-A buck converter using the TPS543C20.*

At no load, the output voltage is the correct 0.85 V. As the output current increases, however, the output voltage drops linearly, as shown in the negative slope of the output voltage vs. load current graph in **Figure 14**.

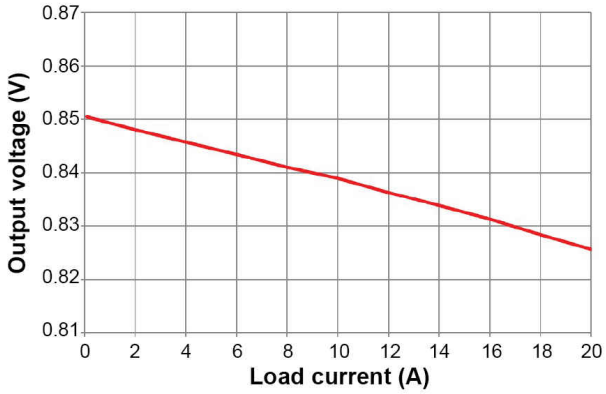

Figure 14. *The output voltage drops linearly at increased loading.*

The purpose of any voltage feedback loop is to keep the potential steady at one point. While a schematic can have an output voltage resistor divider drawn anywhere, the connection on the PCB layout dictates which point the controller regulates. Issues with measurement points are more noticeable in converters with high output current because of the higher voltage drop over a long output voltage plane.

Copper, like any conductor, will have some parasitic resistance based on its length. **Equation 1** simplifies the resistance of a conductor, assuming an equal length and width (see **Figure 15**):

$$R = \frac{\rho \times l}{T \times l} = \frac{\rho}{T} \quad (1)$$

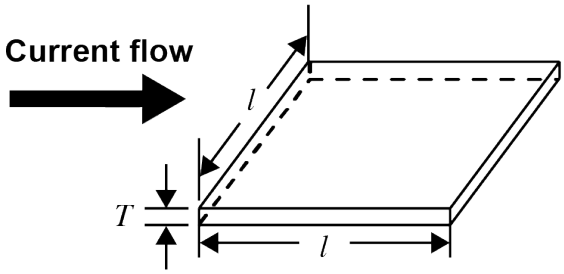

Figure 15. *Conductor simplified with equal length and width.*

Table 1 shows the resistance in milliohms for typical copper thicknesses. When simplifying a long trace into a series connection of squares, multiplying the number of squares by the resistance of a single square gives you the total parasitic resistance of that trace.

Copper Weight (ounces)	Thickness (µm/mils)	Resistance per Square at 25°C (mΩ)	Resistance per Square at 125°C (mΩ)
1/2	17.5/0.7	1	1.4
1	35/1.4	0.5	0.7
2	70/2.8	0.25	0.35

Table 1. *Resistances of typical copper thicknesses.*

Since the PCB was constructed using 2-oz copper, a trace will have roughly 0.35 mΩ per square. The output voltage plane in this design is a little over four squares long. At the copper thickness used, the output plane has 1 mΩ of parasitic resistance in series with the output. Therefore, loading this design to 20 A will create a 20-mV drop across the output plane.

Moving the sense point by the connector eliminates this issue. **Figure 16** shows a corrected layout, with the output voltage sensing trace highlighted in cyan. The green squares illustrate the length of the output voltage trace in squares.

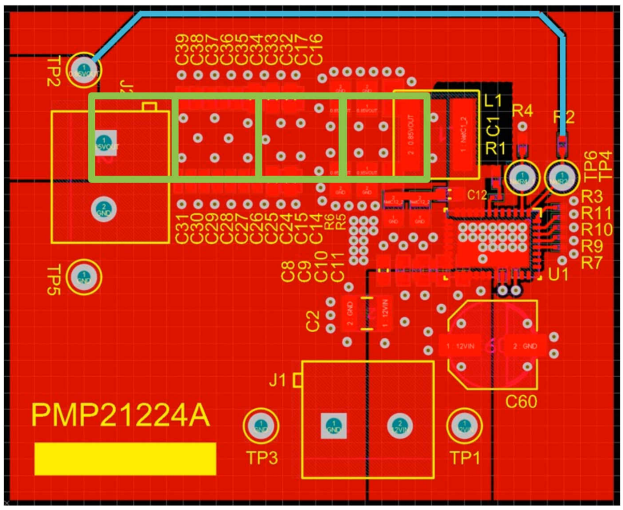

Figure 16. *Output voltage measured at the output connector.*

Having the voltage sense point before the parasitic resistance will lead to regulation inaccuracy at high output currents. **Figure 17** shows a plot of output voltage vs. output current for the two options. The dashed red line correlates to **Figure 14**, where the sense point is before the output plane. Measuring the output voltage by the connector, shown in **Figure 16**, corrects for this loss.

Note the improvement of the solid blue line on **Figure 17** compared to the dashed red line. Proper placement of the output voltage sense can eliminate the effects of parasitic resistance in load regulation.

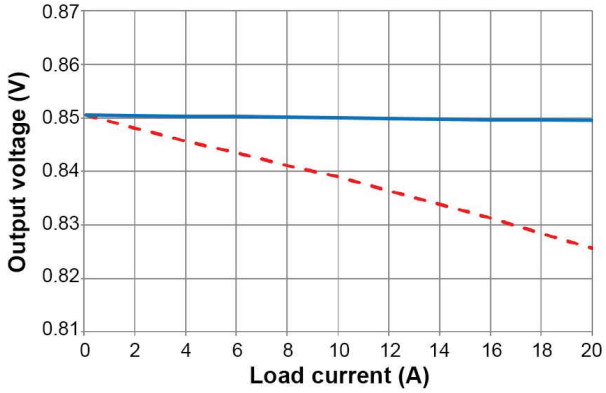

Figure 17. *Sensing the output voltage by the connector improves the output regulation.*

Filter Component Placement

The flyback topology is a low-cost solution to generating an output voltage electrically isolated from the input supply. **Figure 18** shows a simplified schematic of an offline bipolar junction transistor (BJT) flyback converter. The resistor highlighted in green is the filtering resistor placed between the current-sense resistor (red) and the controller integrated circuit (IC) (orange). Placing a resistor between the top of the current-sense resistor and the current-sense pin of the IC can filter out possible switching noise.

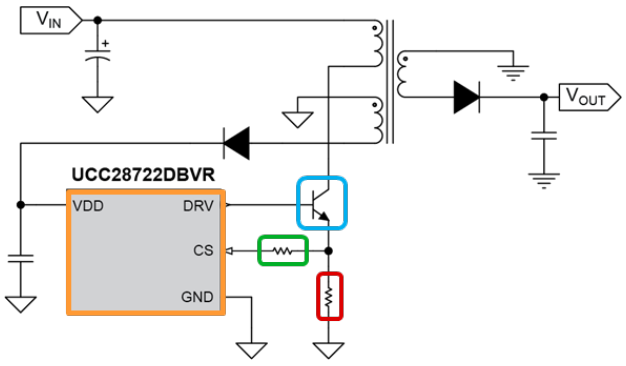

Figure 18. *Simplified schematic of an offline BJT flyback converter.*

Figure 19 is the layout of an isolated flyback design that generates a 3.3-V output capable of 200-mA loading. Something wrong with this layout causes the controller to sense a primary overcurrent fault; the controller goes into overcurrent protection (OCP) before reaching the designed maximum output loading. The colored boxes in the layout of **Figure 19** correlate with the schematic in **Figure 18**.

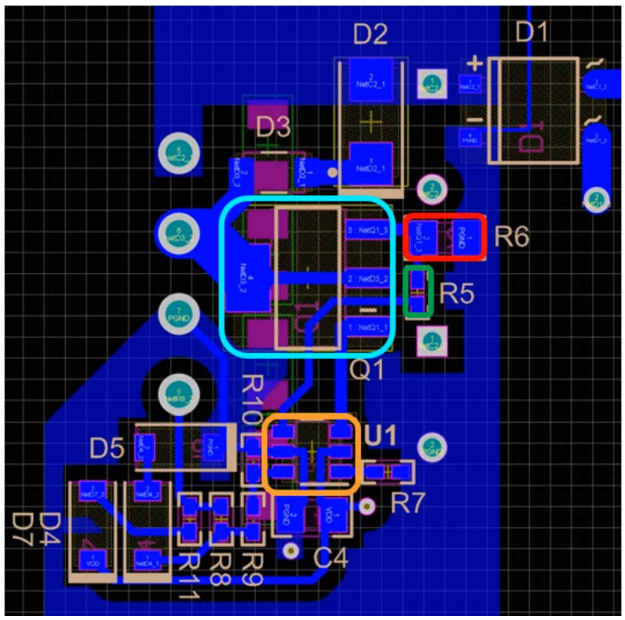

Figure 19. *Flyback controller design.*

The placement of filtering components on the board will affect how well they work. In **Figure 19**, the filtering resistor is placed by the current-sense resistor. This component placement then requires an unreasonably long trace that connects back to the current-sense pin of the IC. A long trace on a sensitive node such as this enables noise to couple into the signal and be measured unattenuated.

The extra noise in this design prevented it from reaching the maximum output current. As the output current increases, the leakage inductance of the transformer captures more energy, which increases the parasitic noise generated on the primary side. This excess noise can couple into the current-sense measurement and cause the OCP to trip prematurely, as illustrated in **Figure 20**.

When the primary BJT switches on, a large spike appears on the front edge of the current-sense waveform (measured at the pin of the IC).

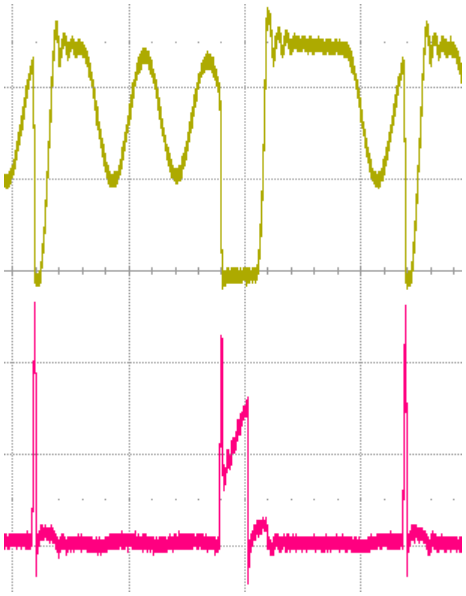

Figure 20. *A leakage spike causes the detection of an OCP fault.*

Proper placement of the filtering resistor can fix this issue. **Figure 21** shows the same converter, but with the filtering resistor placed by the current-sense pin of the IC. Any noise picked up along the current-sense trace is now attenuated before reaching the controller in this design.

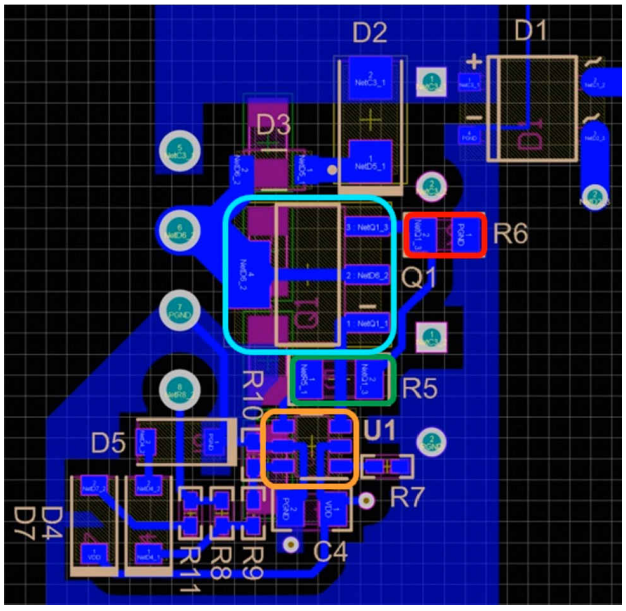

Figure 21. *Filter resistor placed near the controller.*

The result is a controller that does not run into OCP before the output reaches its maximum loading current. **Figure 22** shows the switching and current-sense waveforms of the fixed layout at the maximum output power. While the leading-edge spike is still there, it is attenuated well below the OCP trip point.

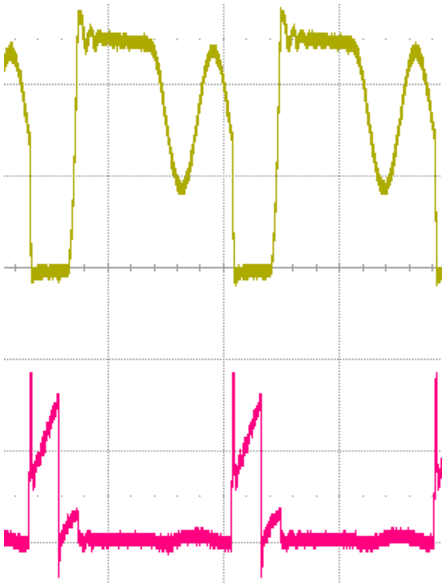

Figure 22. *Waveforms with filter resistor placed near the controller.*

The filter resistor value did not change. Only changing the placement of the resistor mitigated the problem. Additionally, the controller is a quasi-resonant controller with an integrated BJT driver, operating in discontinuous conduction mode. In these waveforms, it appears that the current waveform does not start at zero. This is an artifact of adding the BJT driver current to primary current. The sum of these waveforms will be measured across the current-sense resistor, which makes it appear to be in continuous conduction mode (CCM).

Gate-Driver Placement

Some designs need an external driver to drive the power field-effect transistors (FETs) in a power stage. **Figure 23** is a block diagram for an interleaved CCM power factor correction (PFC) design. The controller IC has two integrated drivers operating 180° out of phase. The power requirements of the design necessitated two power FETs per phase of the PFC.

Adding a dedicated gate-driver IC to the design ensures the driving of both FETs effectively for each phase.

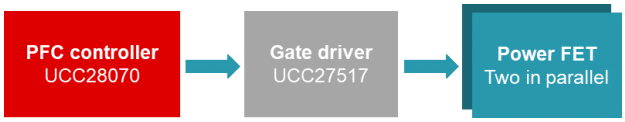

Figure 23. *System architecture for interleaved CCM PFC.*

Figure 24 shows the placement for the system blocks in the first board design for a single phase. The colors in the block diagram correlate to the colors of the circles in the PCB design. There are separate PGND and AGND copper pours that connect together near the controller IC. This design choice helps improve the system's electromagnetic compatibility. The green-shaded layer in **Figure 24** shows the PGND and AGND copper pours.

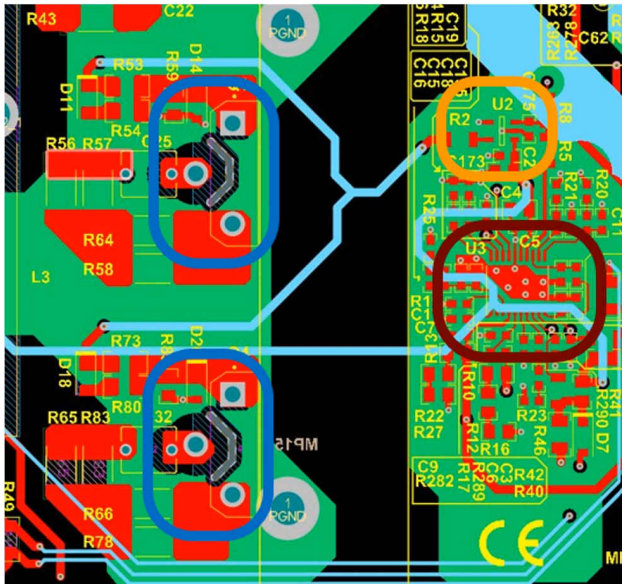

Figure 24. *Initial CCM PFC PCB design.*

This design had a noise issue that was preventing proper driving of the FETs, however. The yellow waveform in **Figure 25** shows the VGS of one of the power FETs during turnoff. While it may not look like much, the "knee" in the VGS waveform shows that the FET is not being driven properly. This issue became more prevalent at a higher output loading, where the FETs were rising in temperature more than expected and eventually failed.

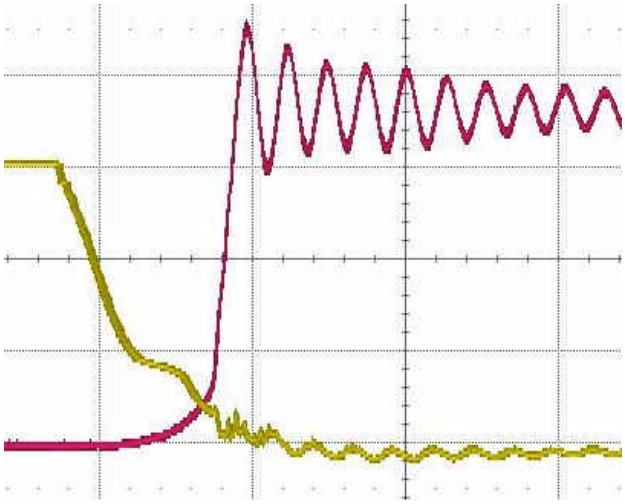

Figure 25. *Notch in VGS waveform (yellow) shows gate-driving issues; VDS (red) shows PFC switching node.*

A gate-drive signal carries both the timing of when to switch as well as the energy required to charge the gate of the FET. Long traces add parasitic resistance and inductance, which reduces the effectiveness of this signal. For this reason, it is important to make the gate-drive trace as short as possible. In designs where the gate driver is separate from the controller, driver placement becomes critical.

The issue with the initial PCB design is the placement of the gate-driver IC. Because of its placement on the AGND side next to the controller IC, the gate-drive signal has to span across the PCB. This long trace is then susceptible to noise and results in a less-effective drive signal. Moving the driver IC to the PGND side of the PCB can eliminate this issue.

Figure 26 shows the PGND section of the second revision of the PCB design. With this system placement, the gate-drive signals, highlighted in cyan, are much shorter compared to the initial design.

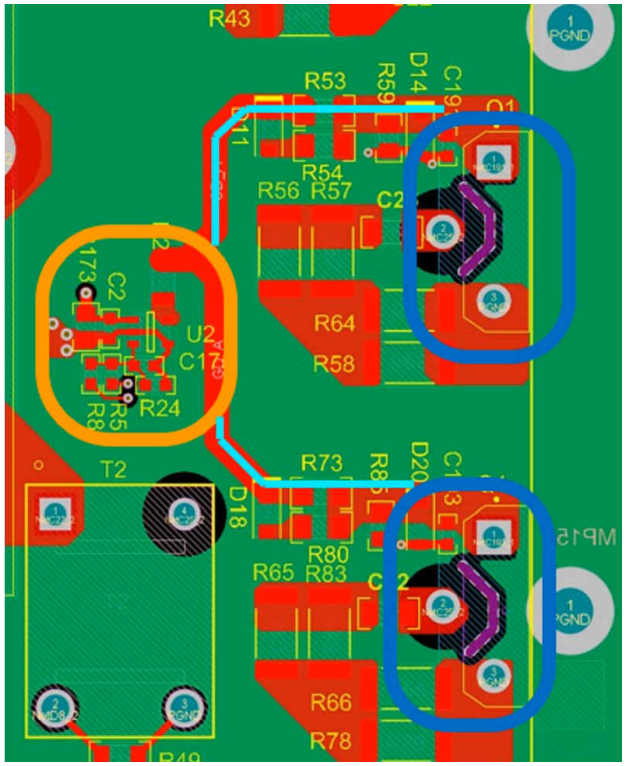

Figure 26. *PGND section of the second PCB design revision.*

The improved layout enables the driver IC to properly switch the power FETs, as illustrated by the clean VGS waveform in **Figure 27**. With a strong gate-drive signal, the design could reach the maximum output power without running into thermal issues.

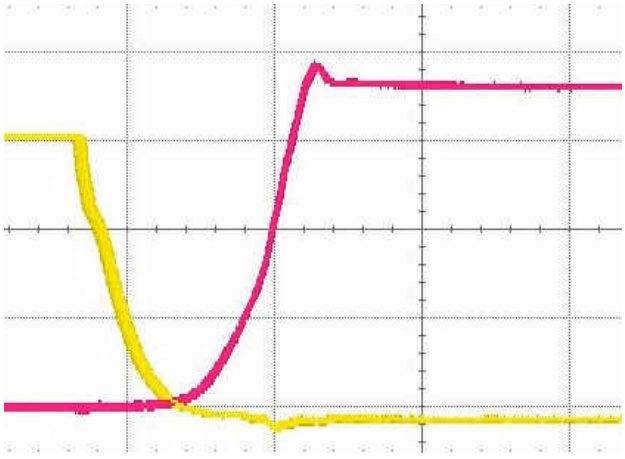

Figure 27. *V_{GS} and switch node in the second PCB design revision.*

The second board revision repositions the gate drivers right next to the power FETs. There is still a gap between the PGND and AGND copper pours; however, in this design the pulse-width modulation (PWM) signal is the trace that spans the gap. A PWM is less susceptible to noise since it does not carry the energy to drive the FET, and there is tolerance for when the rising edge in the signal actuates the driver IC. The additional resilience of this signal allows it to be longer on the PCB without losing functionality.

Thermal Dissipation

Power-converter ICs integrate the power FETs, enabling more compact layouts. And although it is possible to make layouts smaller and smaller, it is still important to carefully plan heat dissipation. Some devices, such as the **TPS54560B** DC/DC converter, use a thermal pad on the bottom of the IC to enable heat to flow from the device to a large copper plane around the IC. Electrically, the thermal pad connects to the ground reference of the IC.

For some topologies, the ground reference of the IC may not be the same as the input to the power supply. One example is an inverting buck-boost converter, where the IC ground and thermal pad connect to the negative output voltage. **Figure 28** shows a design that uses an inverting buck-boost converter with an auxiliary winding to create a positive and negative output voltage. You will need to balance the trade-off between having a larger ground plane or a negative output voltage plane.

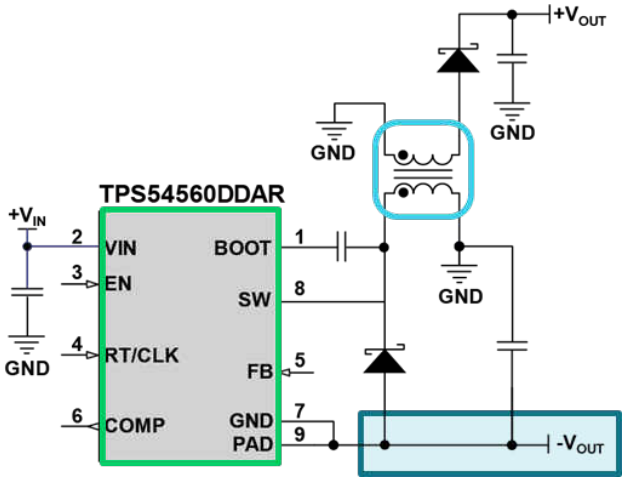

Figure 28. *Schematic of an inverting buck-boost converter with auxiliary winding.*

A larger ground plane will reduce impedance in the return path, which should help noise performance. Making the negative output voltage plane large in this case will provide a larger thermal plane onto which the heat from the IC can spread.

Figure 29 shows a two-layer PCB design that favors a larger, solid ground plane on the bottom. The IC is highlighted in green and the coupled inductor is highlighted in cyan.

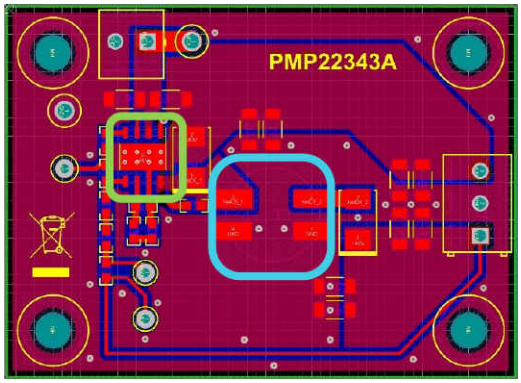

Figure 29. *Design favoring a large ground plane.*

While the large ground plane may have enhanced the electrical performance, the converter IC was heating up. The thermal data in **Figure 30** shows the device heating up more than 60°C over ambient, so the heat is not spreading effectively in this design.

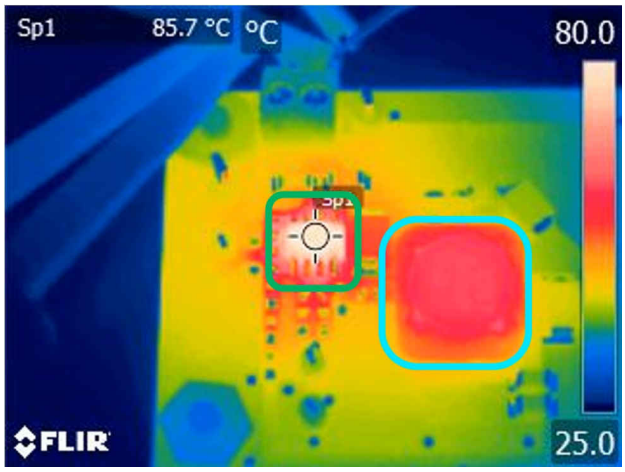

Figure 30. *Thermal data of a design with a large ground plane.*

The design in **Figure 31** has the same schematic, but the PCB has a much larger output voltage plane, achieved by first moving the components on the left side of the IC away from the thermal pad. Next, reducing the size of the ground plane allows for a larger negative output voltage plane. The final adjustment connects the vias under the IC to a large negative output voltage plane on the bottom side of the PCB. The same color scheme identifies both the controller IC and the coupled inductor.

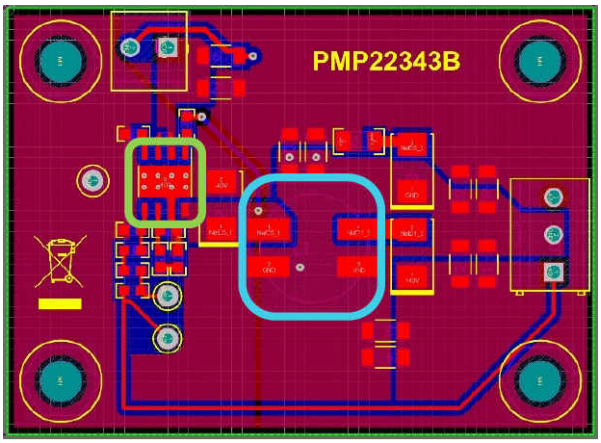

Figure 31. *Design favoring a large output voltage plane.*

Figure 32 shows much-improved thermal performance. Under the same testing conditions, the IC had only a 35°C temperature rise over ambient. Without making the PCB larger or changing the circuit, a better thermal mitigation strategy cut the temperature rise nearly in half.

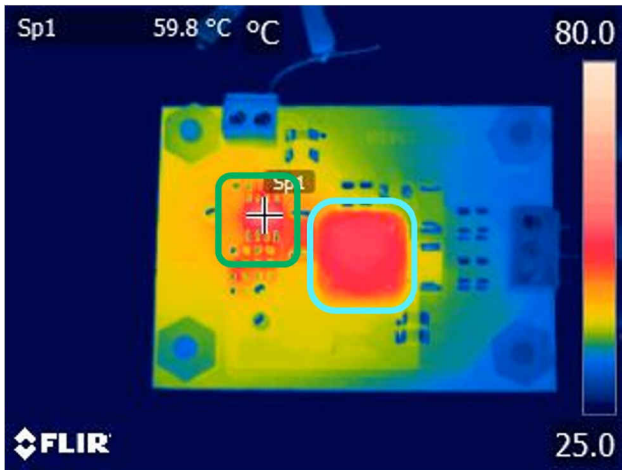

Figure 32. *Thermal data of a design with a large output voltage plane.*

The key to reducing temperature rise is to provide a larger plane for the heat to escape. Minimizing thermal resistance by moving parts out of the way will enable heat to flow more effectively. Physically, this may not always be possible. If too many components need placing around a device with a thermal tab, thermal vias can provide low thermal resistance to a plane on the bottom side of the PCB, as shown in **Figure 33**.

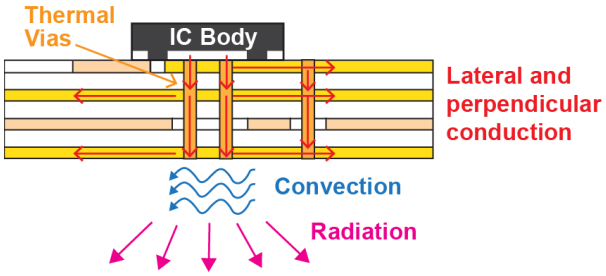

Figure 33. *Using thermal vias to increase the effective surface area of a plane.*

Switch Node Too Large

In the previous layout issue, the power ground and IC reference point were the same node. But what if the FET is external and the IC is not referenced to ground? Should you still make the IC reference node large?

Figure 34 shows a simplified schematic of a high-side buck converter topology.

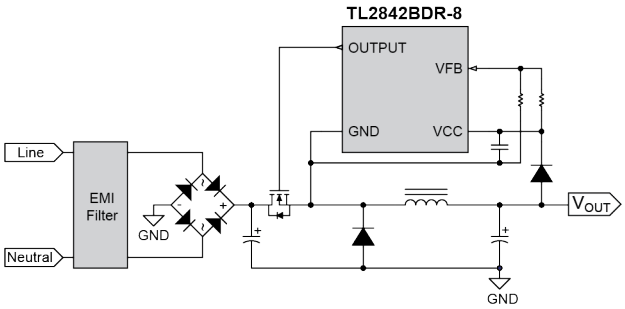

Figure 34. *Simplified schematic of a high-side buck converter.*

The reference for the IC is not the typically quiet ground node but the switch node. The high-side buck topology is mostly used for low-power applications where isolation is not necessary and the input is high voltage. Instead of a customized transformer, an off-the-shelf inductor can reduce cost and complexity [9]. The left side of **Figure 34** shows the EMI filter and diode bridge followed by the power stage. The IC controls the high-side FET.

Figure 35 shows an EMI scan taken during testing of the board. As you can see, the EMI is significant, as the power supply is exceeding the regulatory limits at many points throughout the frequency spectrum.

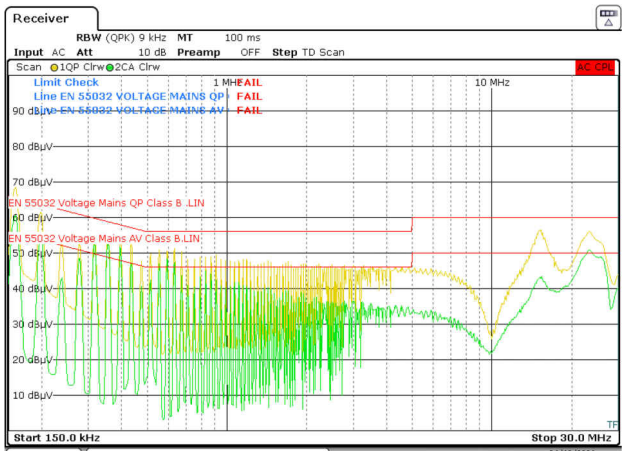

Figure 35. *EMI scan of a high-side buck converter board.*

Changing the EMI filter components did not change the behavior of the scan, hinting that there is an issue with the layout.

Figure 36 is a snapshot of the original layout. The input is on the bottom right, followed by the EMI filter to the left and then the power stage. The control IC and its passives are located on the top right of the board. The output is on the bottom-left side of the board.

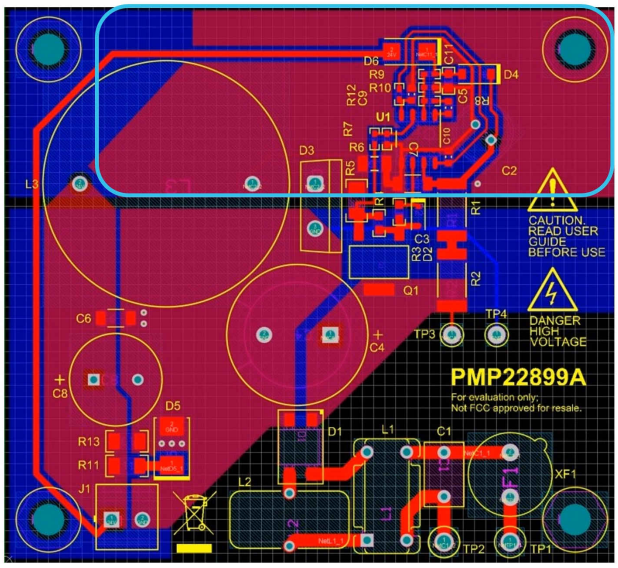

Figure 36. *Original layout of the high-side buck board.*

The cyan box highlights the switch node on the top (red) and bottom (blue) layers. The surface area of the switch node is too large. This node contains high transient voltages (dv/dt) that must be kept to a minimum to minimize parasitic capacitance. Just because this node is the reference for the IC does not mean that it should be any larger. There is minimal power going through the IC because the power stage is external.

Figure 37 shows the new layout (bright) vs. the old layout (dull) in a side-by-side comparison. Notice how much smaller the switch node is. Reducing the switch node to only the top layer and minimizing the copper enabled the pouring of power ground copper on the bottom layer, improving thermal management.

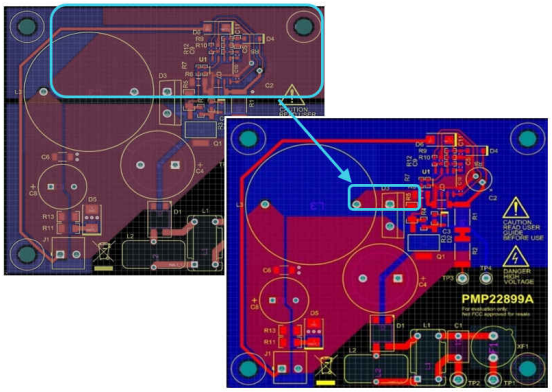

Figure 37. *New layout highlighting the reduction in switch node.*

Figure 38 shows the improved EMI results, which now pass across the entire EMI spectrum.

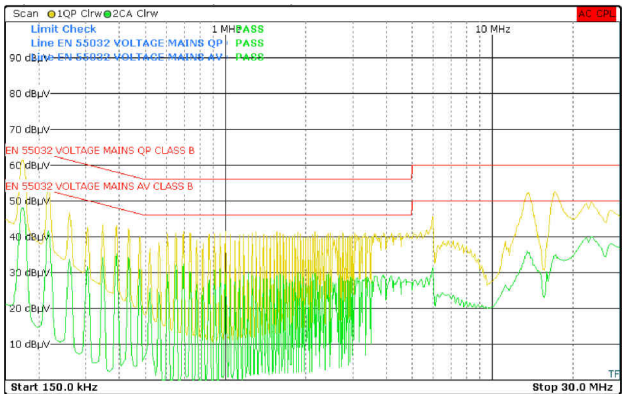

Figure 38. *EMI scan on improved layout.*

A larger surface area of any DC node reduces parasitic resistance and inductance as well as thermal stress, but requires careful planning with high dv/dt nodes such as the switch node. The priority here is the parasitic capacitance, and keeping the surface area as small as possible in order to avoid EMI issues.

Magnetic Component Placement

Beyond optimizing the surface area of a specific node, component placement can also have a positive effect on minimizing the EMI of a power supply. Figure 39 shows a typical isolated flyback design. The input is on the top right, and the EMI filter is highlighted in orange. The isolated power stage with the control IC is located at the bottom left, and the transformer, highlighted in red, is located in the center of the board. The isolated output is located on the bottom right.

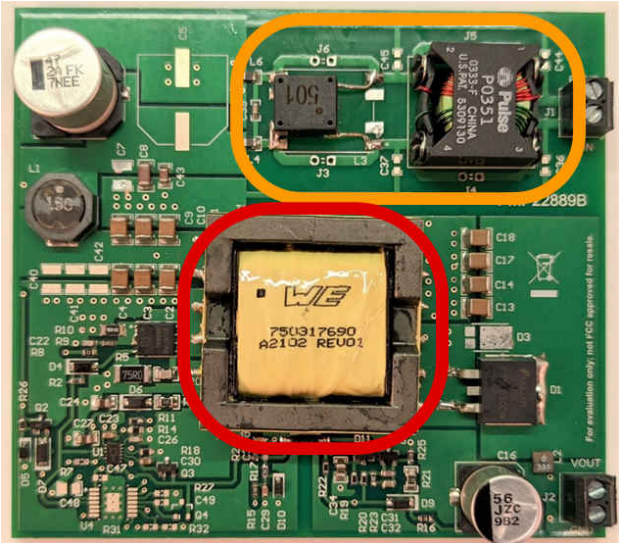

Figure 39. *Offline isolated flyback board.*

The initial EMI scan in **Figure 40** shows that the board is failing at higher frequencies. Failing at these higher frequencies is typically caused by too much common-mode noise in the power supply.

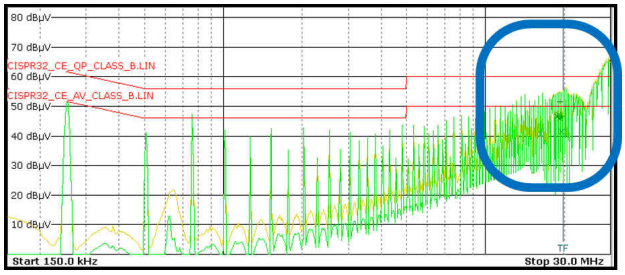

Figure 40. *EMI scan showing high common-mode noise.*

A common-mode choke (CMC) with higher attenuation at these frequencies usually enables the power supply to pass EMI tests, but that did not help here. A CMC with more attenuation had no effect on the EMI scan, as the power supply continued to fail at higher frequencies.

One concern regarding the layout is the proximity of the EMI filter to the transformer. In some layouts, the stray fields from the transformer could couple to the EMI filter components. Using a flux band (a thin piece of copper carefully wrapped all the way around the transformer and then grounded to primary ground) tests this theory, highlighted in cyan in **Figure 41**.

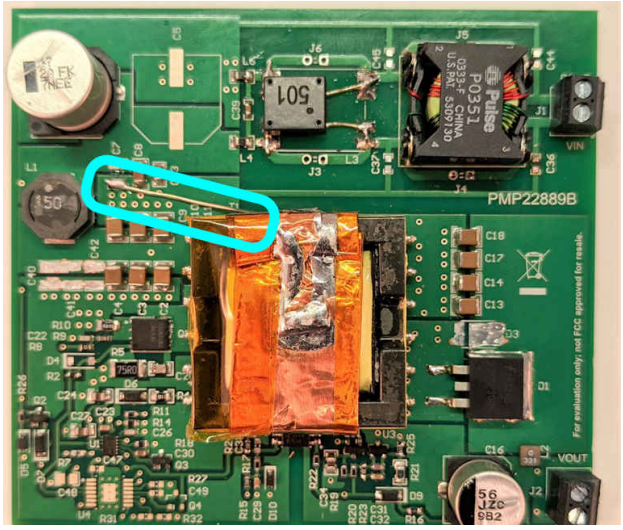

Figure 41. *Flux band wrapped around the transformer and shorted to primary ground.*

Soldering the copper band together forms a shorted turn around the outside of the transformer, shorting out any stray magnetic fields and keeping them from coupling to the components in the EMI filter [**10**]. Grounding the flux band also partially shields electric fields from the core and windings.

Figure 42 illustrates a reduction of 5 dBµV at the higher frequencies, hinting that the transformer may be coupling noise to the EMI filter.

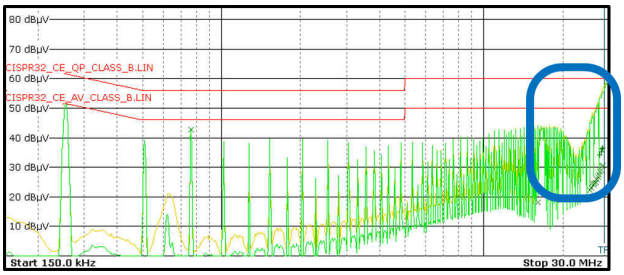

Figure 42. *EMI scan showing a 5-dBµV improvement with flux band.*

For the final solution, the revised layout increases the space between the EMI filter and the transformer. **Figure 43** shows this layout, with the EMI filter (orange) moved far away from the transformer (red).

Figure 43. *Final layout showing the EMI filter further away from the transformer.*

The EMI scan shown in **Figure 44** shows a 10-dBµV reduction with the same CMC and transformer.

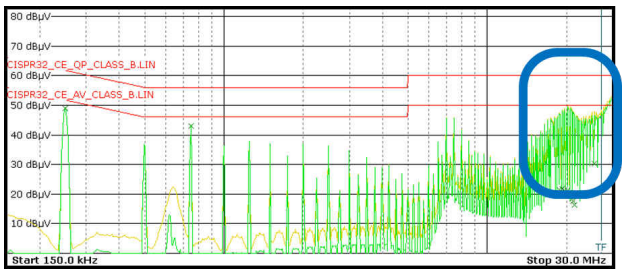

Figure 44. *EMI scan for the revised layout showing a 10-dBµV reduction.*

How was the transformer making the CMC less effective? **Figure 45** offers a side-by-side comparison of both the original and revised layouts, as well as an approximation of the magnetic fields of the transformer indicated with blue ovals.

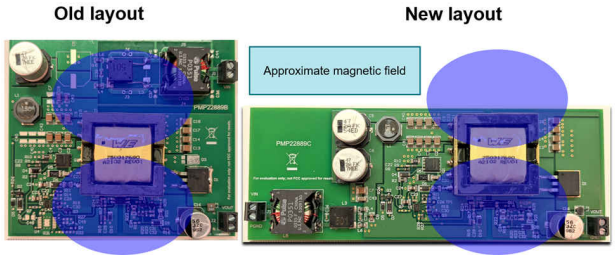

Figure 45. *Side-by-side comparison of original and revised layouts and approximate magnetic fields of the transformer.*

In **Figure 45**, notice the CMC placement at the top right of the original layout, and the green and red windings. Because of the orientation of the transformer's core, the north and south electromagnetic fields generated will couple more to the green winding than the red one. This imbalance will lead to a less-effective filter, and is largely responsible for the noise.

Using a bi-filar CMC, where both wires are wound side by side for tighter coupling between the two CMC windings, can help alleviate this imbalance.

The revised layout also moves the EMI filter far away from the transformer. If moving the filter and transformer is not possible, rotating the transformer to orient the fields to more east and west may also help. Yet another option is to shield the EMI filter using a metal enclosure. When incorporating the flux band as the final solution, confirm that the design does not violate any creepage and clearance safety specifications.

Soft-Shorting Transformer Core

The final power-supply layout mistake to cover has to do with an intermittent problem when there are multiple boards and each board is behaving a little differently. Debugging intermittent issues can be very frustrating. **Figure 46** shows a photo of an AC-to-DC active clamp flyback (ACF) design created for a high-power-density adapter application.

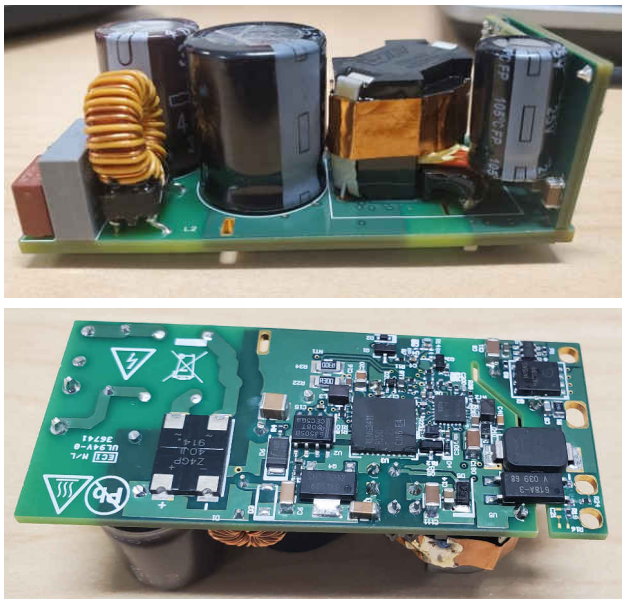

Figure 46. *An AC-to-DC ACF design: profile view (top); bottom view (bottom).*

Meeting electrical specifications without violating any safety specifications in a high-density design requires that you use every square inch of the available space strategically and efficiently.

In this scenario, three boards were each behaving differently:

- The first board was regulating to 5 V and operating regularly.
- The second board was not showing any signs of life.
- The third board was powering up but tripping OCP, as indicated by the scope shot in **Figure 47**.

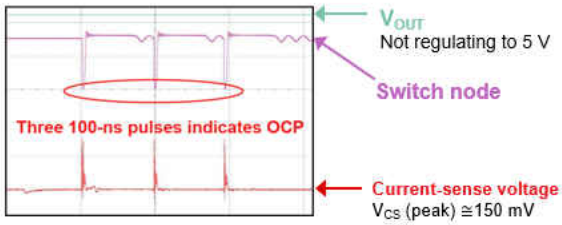

Figure 47. *Three 100-ns pulses on the switch node indicate OCP.*

Inspecting the third board revealed that the current-sense voltage (VCS) was shorting to a 5-V reference voltage (VREF). **Figure 48** is a 3D image of the board layout.

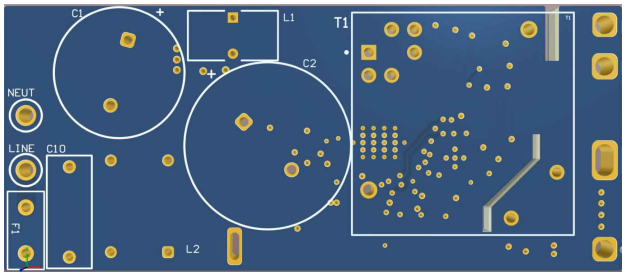

Figure 48. *3D image of the board layout.*

In **Figure 48**, the vias underneath transformer T1 are not thermal vias. They are signal vias used for routing important traces in and around the controller, which is mounted on the bottom side of the board as shown in **Figure 46** (bottom picture). **Figure 46** (top picture) shows that the transformer core is actually touching the board and is soft-shorting the VCS via to the VREF node through the transformer core. Variations in transformer mountings and whether it was touching the board or not explain the intermittent symptoms.

In a space-constrained design such as this one, the IC still needs to make use of the space underneath the transformer, necessitating the need to keep the transformer core from touching the board. Designing a new transformer bobbin (see **Figure 49**) with stand-offs for the existing transformer ensures that the core does not come into contact with the board.

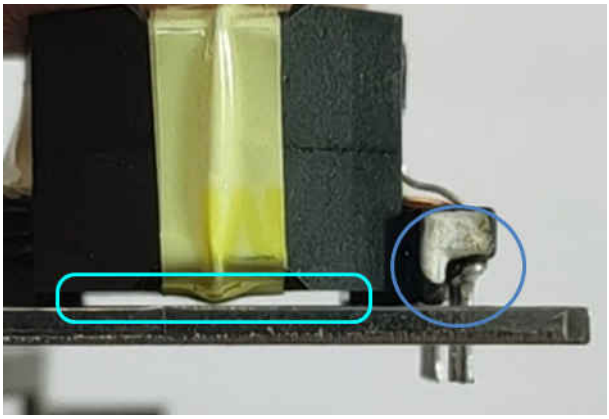

Figure 49. *New transformer bobbin showing stand-offs (blue) to give clearance underneath (cyan) (Source: Renco Electronics Inc.).*

It is usually not a best practice to route anything under magnetics, but in super-tight designs, it is sometimes unavoidable. There are other ways to avoid potential problems when routing under the transformer, such as using insulating tape to wrap the transformer and creating a barrier between the transformer and the board, as shown in **Figure 50**.

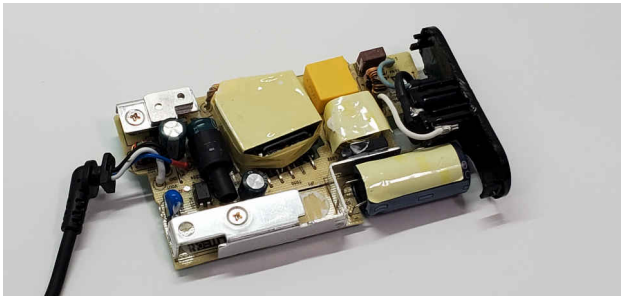

Figure 50. *A transformer wrapped with insulating tape helps avoid any short circuits underneath.*

For non-isolated designs that have tight space constraints, using raised inductors (see **Figure 51**) can be very useful. Mounting components directly underneath the inductor can help make the design as small as possible.

Figure 51. *Raised inductors in a non-isolated design (Source: Coilcraft Inc.).*

Conclusions

While these may be some of the most common power-supply layout mistakes, there are still others. Every layout is different, but what remains consistent is that in order to produce a good layout, you must understand the circuit fully and the environment or application that the board will be a part of.

Carefully consider each block of components on the schematic, whether they are there for safety, EMI, feedback, thermal relief, and so on.

Before starting the layout, ask yourself some essential questions about the schematic. Where are the high-current paths? Which nodes are high transient current or high dv/dt nodes? Where are the feedback components? Which components in the power stage will need thermal relief? How many layers do you have to work with to dissipate the heat? How will you accomplish the grounding? Preparing with this level of detail before starting will help ensure that you have a successful layout with minimal issues.

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